CLAIMS

1. A semiconductor device comprising:

a semiconductor substrate comprising a top surface and a bottom surface;

a plurality of active regions formed in said top surface;

a plurality of blind features disposed in said bottom surface; and

a material deposited on surfaces of said blind features, wherein an electrical conductivity of said material is greater than an electrical conductivity of said semiconductor substrate.

2. The semiconductor device of Claim 1, wherein a thermal conductivity of said material is greater than a thermal conductivity of said semiconductor substrate.

3. The semiconductor device of Claim 1, wherein said material partially fills each of the blind features.

4. The semiconductor device of Claim 1, wherein said material completely fills each of the blind features.

5. The semiconductor device of Claim 1, wherein said semiconductor substrate comprises a material selected from the group consisting of silicon, germanium, and III-V compounds.

6. The semiconductor device of Claim 1, wherein said material comprises a metal.

7. The semiconductor device of Claim 1, wherein said material comprises a filled polymer.

8. The semiconductor device of Claim 1, further comprising an epitaxial layer disposed between said active regions and said substrate and wherein a depth of said blind features is equal to a thickness of said substrate.

9. The semiconductor device of Claim 1, further comprising at least two parasitic bipolar transistors, and wherein at least one of said blind features is disposed in proximity to one of said parasitic bipolar transistors.

10. The semiconductor device of Claim 9, further comprising:

an N-well disposed in said top surface;

a PFET disposed in said N-well; and

an NFET disposed in said top surface.

11. A semiconductor wafer comprising:

a semiconductor substrate comprising a top surface and a bottom surface;

a plurality of active regions formed on said top surface wherein said active regions are separated by a plurality of streets; and

a plurality of street grooves disposed on said bottom surface of said semiconductor substrate, wherein said street grooves are aligned opposite said plurality of streets.

12. The semiconductor wafer of Claim 11, further comprising:

a plurality of blind features disposed in said bottom surface; and

a material deposited on surfaces of said blind features, wherein an electrical conductivity of said material is greater than an electrical conductivity of said semiconductor substrate.

13. The semiconductor device of Claim 12, wherein a thermal conductivity of said material is greater than a thermal conductivity of said semiconductor substrate.

14. The semiconductor device of Claim 12, wherein said material partially fills each of the blind features.

15. The semiconductor device of Claim 12, wherein said material completely fills each of the blind features.

16. The semiconductor device of Claim 12, wherein said semiconductor substrate comprises a material selected from the group consisting of silicon, germanium, and III-V compounds.

17. A method for processing a semiconductor wafer comprising:

applying a mask to a back side of said wafer;

etching a plurality of blind features into said back side of said wafer; and

depositing a material on surfaces of said blind features, wherein an electrical conductivity of said material is greater than an electrical conductivity of said semiconductor wafer.

18. The method of Claim 17, wherein a thermal conductivity of said material is greater than a thermal conductivity of said semiconductor substrate.

19. The method of Claim 18, wherein said material completely fills each of the blind features.

20 The method of Claim 17, further comprising:

applying a street mask to said back side of said wafer; and

etching a street groove pattern in said back side of said wafer, wherein said street groove pattern is aligned with a street pattern on a front side of said wafer.